PUCC3801

Current-mode PWM controller

Rev. 01 — 10 September 2001 **Product data**

1. General description

The PUCC3801 is a current-mode Pulse Width Modulated (PWM) controller containing all the control and protection functions necessary to implement an off-line, flyback or forward converter with a minimum number of external components.

2. Features

- Very low start-up supply current; 50 μA typical
- Low operating supply current; 1.2 mA typical
- Accurate, internally-trimmed, fixed frequency oscillator (100 kHz). No external timing components needed
- Internal slope compensation. No external ramp components needed
- Built-in over-voltage and under-voltage detection
- High-speed over-current trip; 170 ns typical
- Over-voltage clamp on supply voltage (V_{DD})
- Internal divider regulates V_{DD} to 12 V. No external divider needed
- Leading edge blanking of the current sense signal
- Control frequency modulated over a narrow band to reduce Electromagnetic Interference (EMI)
- High output drive capability; 150 ns typical rise and fall time into 2 nF load
- Wide bandwidth (10 MHz) error amplifier with external compensation pin and simple interface to optocoupler
- Accurate internal bandgap reference.

3. Applications

- Off-line switched mode power supplies
- Laptop computer mains adaptors
- Printer power supplies.

PHILIPS

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PUCC3801P	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
PUCC3801T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

5. Block diagram

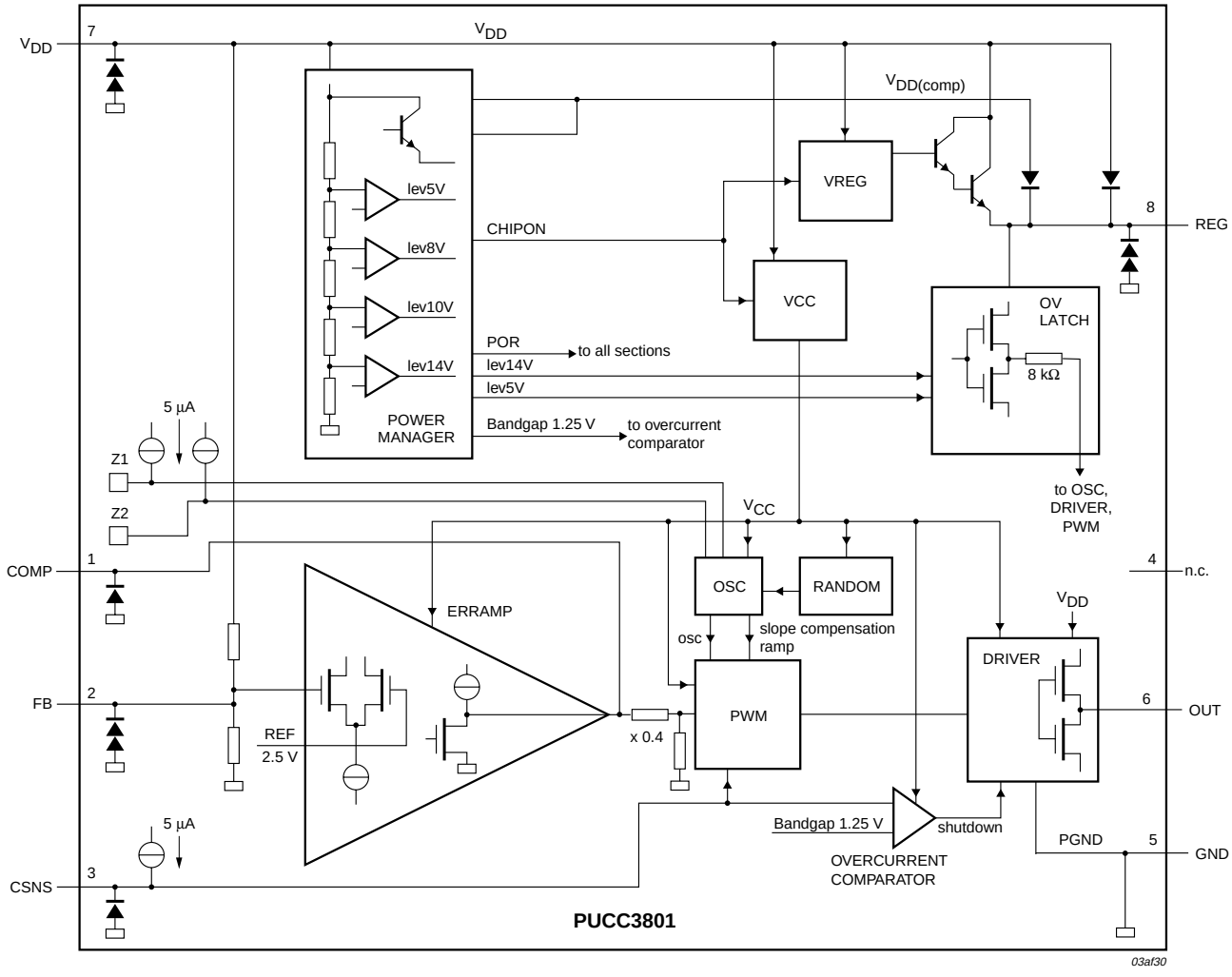


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

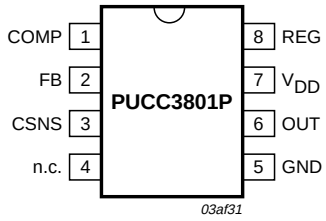


Fig 2. Pin configuration; PUCC3801P (SOT97-1).

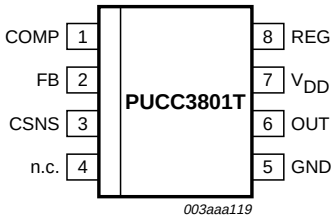


Fig 3. Pin configuration; PUCC3801T (SOT96-1).

6.2 Pin description

Table 2: Pin description

Symbol	Pin	I/O	Description
COMP	1	I/O	compensation pin
FB	2	I	feedback pin
CSNS	3	I	current sense input
n.c.	4	–	no connection
GND	5	–	circuit common ground
OUT	6	O	gate drive output
V_{DD}	7	–	positive supply voltage
REG	8	O	voltage regulator decoupling pin

7. Functional description

7.1 Pin functions

7.1.1 Compensation pin (COMP)

The compensation pin is connected to the output of the error amplifier (ERRAMP). This pin is normally connected via a feedback network to the FB pin. The COMP pin can also be used as an input for an optocoupled control signal to the pulse width modulator (PWM) comparator. When an optocoupler is used, the collector of the optocoupler photo-transistor is connected to the COMP pin, with a pull-up resistor to V_{DD}. The FB pin must be grounded to force the output of the error amplifier HIGH.

7.1.2 Feedback pin (FB)

The feedback (FB) pin is the inverting input to the error amplifier. If FB is left open, an internal divider from V_{DD} will tend to regulate V_{DD} at a nominal 12 V.

7.1.3 Current sense input pin (CSNS)

The signal on the current sense input pin is connected to the input of the pulse width modulator comparator. A low pass filter suppresses transients and noise on the leading edge of the current sense signal. Inside the PWM, a slope compensation ramp, derived from the main oscillator (OSC) is added to the current sense signal. The internal slope compensation feature allows stable operation of the converter at duty cycles greater than 50%.

The signal on the current sense input pin is also connected to the input of an over-current comparator. If the amplitude of the current sense signal exceeds 1.25 V, the comparator detects an overload condition and immediately terminates the output pulse. The propagation delay from CSNS to output, in an over-current condition, is typically 170 ns.

7.1.4 Common circuit ground pin (GND)

This is the common power and signal ground connection. The power and signal grounds are separated internally for improved noise immunity.

7.1.5 Gate drive output pin (OUT)

When no output pulses are being produced, this pin is held LOW. An external pull-down resistor on the MOSFET gate is not required.

7.1.6 Positive supply voltage pin (V_{DD})

An internal shunt regulator allows the device to be powered via a resistor from a widely varying supply. The device power management section keeps the device in start-up current mode whilst V_{DD} is ramping up. When the supply voltage reaches the start-up threshold, the device turns on and draws the specified supply current. If V_{DD} drops below the under-voltage lockout threshold, the device returns to start-up current mode.

7.1.7 Voltage regulator pin (REG)

This is a decoupling pin for the internal low voltage supply (V_{REG}). This pin must not be loaded during start-up or whilst the device is in start-up current mode.

7.2 Device sections

The device can be considered as two sections (see Figure 1):

- **Power-up section** consisting of the POWER MANAGER, VREG, VCC, OV LATCH and $VDD_{(comp)}$ circuitry. This part is always active.
- **Controller section** consisting of the ERRAMP, PWM, DRIVER, OSC, RANDOM and OVERCURRENT COMPARATOR. This part is supplied by an internally generated 5 V supply (V_{CC}), controlled by the power-up section. The controller section is kept switched off during power-up to minimize the start-up current.

7.2.1 Power-up section

Power-up sequence: The power-up sequence disables the controller section and keeps the start-up current below 70 μA until V_{DD} rises above 10 V.

With reference to Figure 4, assume that V_{DD} is rising slowly from zero to 12 V. The Power Manager produces a Power-On Reset (POR) signal that is routed to every flip-flop and counter in the device. This signal is made active as early as possible in the power-up sequence to ensure that the internal logic is reset and the device powers up in a known state.

The POR remains active until the bandgap reference voltage ($V_{bandgap}$) stabilizes and the comparators in the power manager block have all settled into stable states. The POR signal is then released and, once the supply voltage, V_{DD} reaches 10 V, the controller section is enabled and the device starts to produce output pulses.

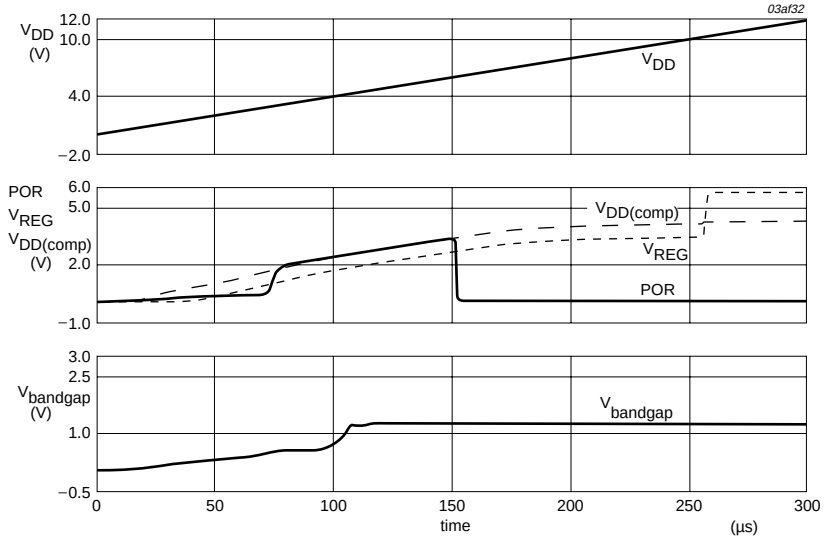


Fig 4. Power-up sequence.

Over-voltage and under-voltage functions: Figure 5 shows the over-voltage trip sequence.

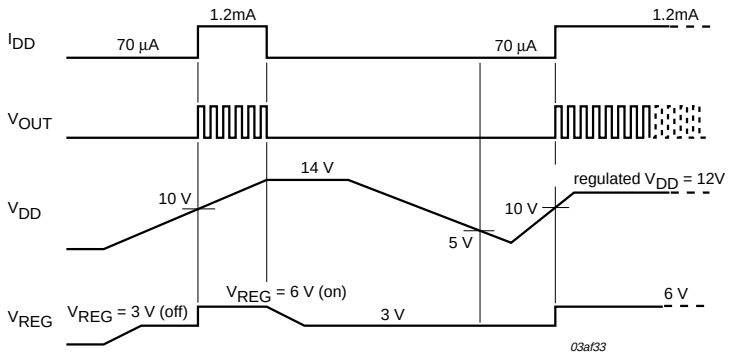


Fig 5. Over-voltage and under-voltage functions.

A coarse internal supply V_{REG} is generated by the VREG section. In standby mode, this supply drops to a low level, typically 3 V, and the current into the V_{DD} pin is limited to a low value, less than 70 µA.

When V_{DD} rises above 10 V, V_{REG} rises to 6 V and the operating supply current increases to typically 1.2 mA. The device starts normal operation and output pulses are produced.

The over-voltage trip sequence is initiated if V_{DD} rises above 14 V. When this happens, the output pulses are disabled, V_{REG} is reduced gradually to 3 V, and the output of the over-voltage latch goes HIGH.

The device remains in the over-voltage lockout mode until V_{DD} falls below 5 V.

Input voltage clamp: V_{DD} is clamped to a maximum of 16.5 V. The size of the external resistor must be sufficient to ensure that the current into the V_{DD} pin never exceeds 15 mA.

7.2.2 Controller section

Oscillator: The internal oscillator generates a 75% duty cycle digital clock to the output latch, and a 100 kHz voltage ramp to the PWM circuit. The frequency is modulated by approximately 20% by a Pseudo Random Binary Sequence (PRBS) that repeats every 15 cycles. This spreads the electromagnetic interference produced by the power supply over a narrow band of frequencies centered on 100 kHz. This reduces the amplitude of the harmonics in the interference spectrum.

Error amplifier: This section senses one of the various feedback methods used to control the output duty cycle. It contains an operational transconductance amplifier (ERRAMP), that can be externally compensated at the COMP pin. The reference input of ERRAMP is connected to a 2.5 V reference voltage. The FB input is internally connected to a voltage divider from V_{DD}. If the FB pin is not connected, the device will tend to regulate V_{DD} to 12 V.

The output of the error amplifier is connected to the PWM section by a voltage divider with a gain of 0.4 and an output impedance of 100 kΩ.

PWM: The PWM section includes a current sense input from the CSNS pin, a low-pass filter, summing amplifier, a high-speed comparator and logic. This section sums the analog ramp from the oscillator with the voltage on the CSNS pin. This signal is fed to a comparator that triggers on the falling edge of the PWM clock signal. This provides line compensation and load regulation. The internal slope compensation function removes the need for external components to generate a ramp signal that is added to the current sense signal.

A fast over-current path is provided from CSNS to OUT with a typical propagation delay of 170 ns.

Output driver: This section is a high-speed, high-current output stage capable of driving the gate of a large power FET. Typical rise and fall times are 160 ns and 150 ns respectively into a 2 nF load.

8. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage	$I_{DD} \leq 15$ mA	–	15	V
		low impedance source	–	13	V
V_{COMP}	voltage on COMP pin		–0.3	V_{REG} + 0.3	V
V_{FB}	voltage on FB pin		–0.3	V_{REG} + 0.3	V
I_{DD}	supply current into V_{DD} pin		–	15	mA
I_{ORM}	repetitive peak output current		–	0.6	A
I_{REG}	current out of REG pin		–	10	mA
I_{COMP}	current into COMP pin		–	1	mA
P_{tot}	total power dissipation				
	PUCC3801P		–	0.5	W
	PUCC3801T		–	0.3	W
T_j	junction temperature		0	105	°C
T_{stg}	storage temperature	non-operating	–60	+150	°C
T_{sp}	solder point temperature	during soldering; t ≤ 10 s	–	300	°C

9. Characteristics

Table 4: Characteristics

V_{DD} = 12 V; CSNS = LOW; C_{load} = 2000 pF; C_{REG} = 100 nF (REG to GND); T_{amb} = 0 to 105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply current						
$I_{DD(su)}$	start-up supply current into V_{DD} pin	$V_{DD} \leq 9$ V	20	50	70	µA
$I_{DD(oper)}$	operating supply current into V_{DD} pin	V_{DD} = 12 V; no load on other pins	0.5	1.2	4	mA
Supply voltage and over-voltage function						
$V_{DD(th)su}$	start-up threshold voltage	V_{DD} increasing; V_{REG} > 5 V	9	10	11	V
$V_{DD(th)uv}$	under-voltage threshold voltage	V_{DD} decreasing; V_{REG} < 5 V	7.6	8	8.4	V
$V_{DD(th)ov}$	over-voltage threshold voltage	V_{DD} increasing; OV latch output = HIGH	13	14.2	14.7	V
		V_{DD} decreasing; OV latch output = LOW	–	5	–	V
V_{hys}	hysteresis		–	2	–	V
$V_{DD(clamp)}$	clamping voltage	I_{DD} = 10 mA; no load on other pins	13	14.8	16.5	V

Table 4: Characteristics *...continued*

V_{DD} = 12 V; CSNS = LOW; C_{load} = 2000 pF; C_{REG} = 100 nF (REG to GND); T_{amb} = 0 to 105 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Low voltage regulator							
V_{REG}	regulator voltage	I_{REG} = −1 mA		5.5	5.7	7	V
		I_{REG} = −5 mA; V_{DD} = 7.6 V		5	5.4	–	V
		I_{REG} = −10 mA; V_{DD} = 7.6 V		4.5	5.0	–	V
		over-voltage condition		2.8	3.2	4.4	V
$V_{bandgap}$	bandgap voltage	I_{REG} = −1 mA		–	1.25	–	V
Oscillator							
$T_{AV(osc)}$	average period	8.4 V < V_{DD} < 13 V; 15 cycle average	[1]	9.3	10.0	10.7	µs
N_{rep}	modulation repetition number of cycles		[1]	–	15	–	cycles
$\frac{\Delta T_{(osc)}}{T_{AV(osc)}}$	modulation (peak-to-peak value)		[1]	17	20	23	%
δ_{max}	maximum duty factor	V_{COMP} = 4 V	[1]	70	75	80	%
$t_{W(min)}$	minimum pulse duration	V_{CSNS} = 0 V; V_{COMP} = slope compensation stop voltage	[1]	500	–	–	ns
Error amplifier							
$V_{i(ref)(FB)}$	non-inverting input reference voltage	V_{COMP} = 12 V; FB connected to COMP	[2]	2.37	2.5	2.62	V
$R_{i(FB)}$	input resistance at FB pin	from FB pin to GND		–	100	–	kΩ
$V_{DD(reg)}$	V_{DD} regulation voltage	FB pin open		11.4	12	12.6	V
G_{ol}	open-loop gain	no load on COMP pin		65	75	85	dB
GB	gain bandwidth product	no load on COMP pin		–	10	–	MHz
$V_{OH(COMP)}$	HIGH-level output voltage at COMP pin	V_{FB} = 2 V		4.5	5.1	–	V
$V_{OL(COMP)}$	LOW-level output voltage at COMP pin	V_{FB} = 3 V		–	65	250	mV
$I_{O(source)}$	output source current out of COMP pin	V_{COMP} = 3 V; V_{FB} = 2 V		−100	−50	−25	µA
$I_{O(sink)}$	output sink current into COMP pin	V_{COMP} = 1 V; V_{FB} = 3 V		125	300	500	µA

Table 4: Characteristics *...continued*

V_{DD} = 12 V; CSNS = LOW; C_{load} = 2000 pF; C_{REG} = 100 nF (REG to GND); T_{amb} = 0 to 105 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Current sense comparator							
$\frac{V_{CSNS}}{V_{COMP}}$	scaling of CSNS voltage to COMP voltage		[3]	–	40	–	%
$Z_{i(CSNS)}$	input impedance at CSNS pin	f_{in} = 1 MHz		–	100	–	kΩ
τ_{filter}	input filter time constant			–	320	–	ns
$t_{PD(PWM)}$	propagation delay from CSNS to OUT via PWM	V_{COMP} = 1.4 V; V_{CSNS} = 1V pulsed	[4]	–	300	–	ns
$V_{SC(start)}$	slope compensation start voltage	V_{CSNS} = 0 V; duty cycle = maximum	[5]	2.2	2.4	2.6	V
$V_{SC(stop)}$	slope compensation stop voltage	V_{CSNS} = 0 V; no output pulses	[5]	0.3	0.5	0.6	V
Over-current sense comparator							
$V_{th(CSNS)}$	comparator threshold voltage at CSNS pin	V_{FB} = 2 V		–	1.25	–	V
$t_{PD(OC)}$	propagation delay from CSNS to OUT via over-current comparator	V_{COMP} = 4 V; V_{CSNS} = 1.65 V; pulsed	[6]	–	170	250	ns
Output							
V_{OL}	LOW level output voltage	I_{OUT} = 10 mA		–	0.06	1.7	V
V_{OH}	HIGH-level output voltage	V_{DD} = 12 V		–	V_{DD}	–	V
R_{OH}	HIGH-level output resistance	V_{DD} = 12 V; I_{OUT} = 10 mA		30	65	90	Ω
R_{OL}	LOW-level output resistance	V_{DD} = 12 V; I_{OUT} = 10 mA		1	7	14	Ω
$t_{o(r)}$	output rise time	C_L = 2 nF; 10% to 90%	[7]	60	160	260	ns
$t_{o(f)}$	output fall time	C_L = 2 nF; 90% to 10%	[7]	50	150	250	ns

[1] Measured at OUT pin.

[2] Measured at COMP pin.

[3] The amplifier output is connected to the PWM section by a voltage divider with a gain of 0.4 and an impedance of 100 kΩ.

[4] The propagation delay is measured from the 50% point on the CSNS input voltage to the 90% point on the falling edge of the output pulse. A HIGH of 1 V is generated on CSNS after every rising edge of V_{OUT}.

[5] With CSNS tied to ground, the duty cycle can be controlled by varying the voltage on COMP. $V_{SC(start)}$ is the voltage on COMP that produces maximum duty cycle. $V_{SC(stop)}$ is the voltage on COMP at which the output pulses disappear.

[6] The propagation delay is measured from the 50% point on the CSNS input voltage to the 90% point on the falling edge of the output pulse. A HIGH of 1.65 V is generated on CSNS after every rising edge of V_{OUT}.

[7] These limits are not guaranteed. The values are based on simulation results only.

10. Application information

10.1 Off-line flyback regulator

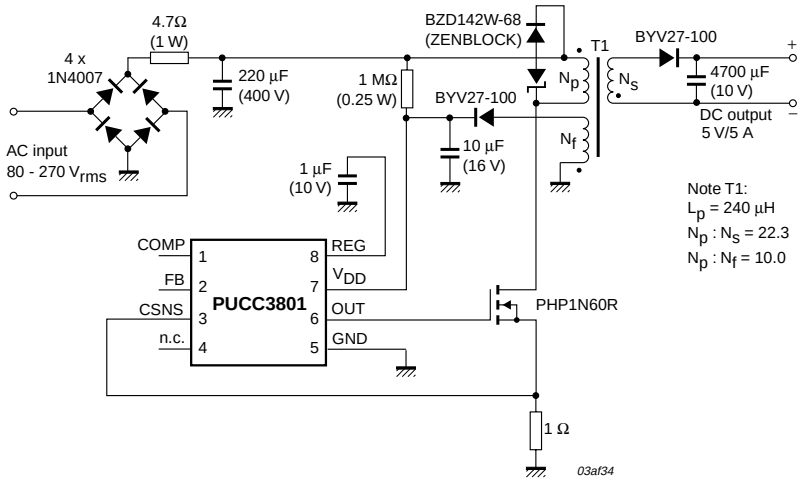


Fig 6. Off-line flyback regulator.

Figure 6 shows a typical application diagram of a low-cost, off-line, flyback regulator. The circuit uses a minimum number of external components. The PUCC3801 has an internal voltage divider from V_{DD}. When the FB pin is left open circuit, the circuit regulates V_{DD} at 12 V. Load regulation is dependent upon close coupling between the secondary and feedback windings, and the leakage inductance of the transformer.

The circuit is designed to operate over the input voltage range 90 - 270 V (RMS). The low start-up current of the PUCC3801 means that the dissipation in the 1 MΩ, 0.25 W resistor to V_{DD} does not become excessive at high input voltages. The internal slope compensation allows stable operation at low input voltage and maximum load where the duty cycle is greater than 50%.

10.2 Optocoupler interface

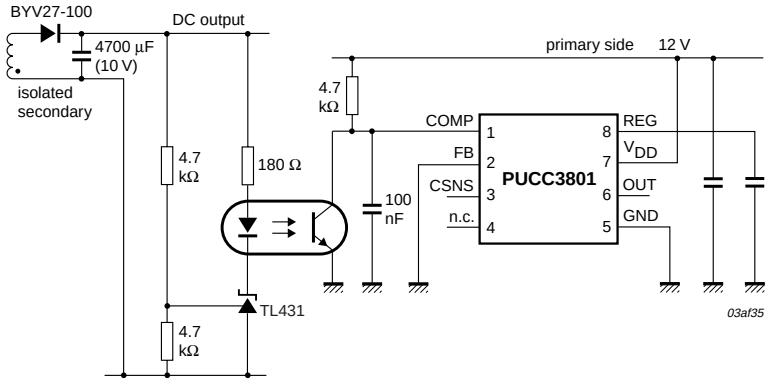
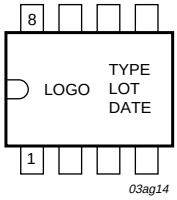


Fig 7. Optocoupler interface to PUCC3801.

Figure 7 shows the method of interfacing an optocoupler to the PUCC3801. The error amplifier is overridden by holding the FB pin LOW. This causes the output of the error amplifier to go HIGH. In this state, the amplifier sources a constant current of typically 50 μA into the collector of the optocoupler. The pull-up resistor to V_{DD} sets the saturation current of the optocoupler transistor.

The secondary side circuit using the TL431 adjustable precision shunt regulator, is a widely used technique not specific to the PUCC3801. The 180 Ω resistor biases the TL431 in its linear region. If the output voltage rises above the regulation point, the TL431 draws current through the optocoupler causing the voltage on COMP to fall. As the voltage on COMP falls, the duty cycle is reduced bringing the secondary voltage back to its set point.

11. Marking

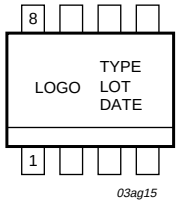


TYPE: PUCC3801P

LOT: Diffusion lot number (5 characters)

DATE: Die revision (1 character) + Date code (yyww)

Fig 8. Marking PUCC3801P (SOT97-1).



TYPE: CC3801T

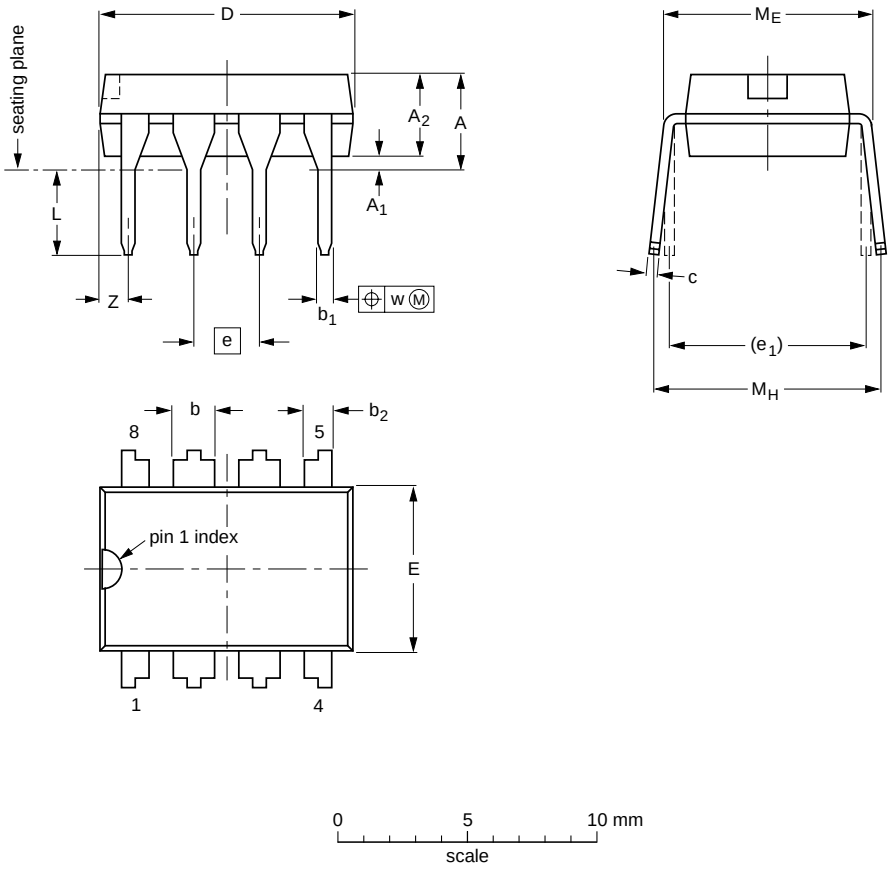
LOT: Diffusion lot number (5 characters)

DATE: Die revision (1 character) + Date code (yyww)

Fig 9. Marking PUCC3801T (SOT96-1).

12. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

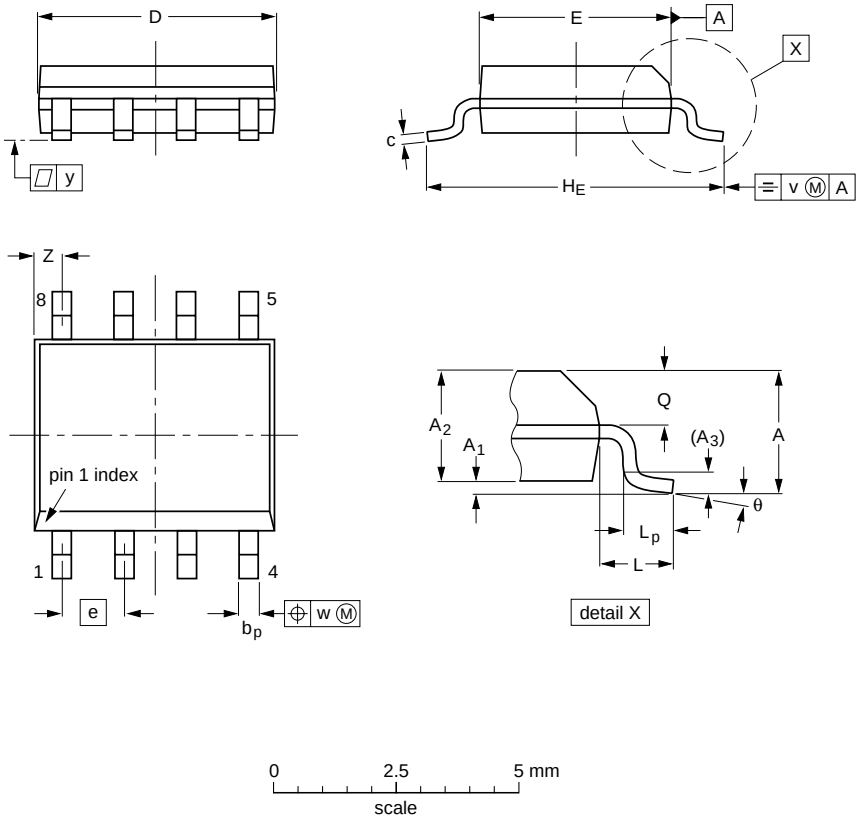
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001	SC-504-8			~~95-02-04~~ 99-12-27

Fig 10. SOT97-1 (DIP8) package outline.

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				~~97-05-22~~ 99-12-27

Fig 11. SOT96-1 (SO8) package outline.

13. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20010910	-	Product data; initial version

14. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

15. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

16. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Contact information

For additional information, please visit **http://www.semiconductors.philips.com**.
For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**. **Fax: +31 40 27 24825**

9397 750 08419

Contents

Date of release: 10 September 2001 **Document order number: 9397 750 08419**